

Verification and Repair of a Space-Efficient Quantum ECDLP Construction

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Abstract

Luo et al. propose an 835-logical-qubit circuit for the elliptic-curve discrete-logarithm problem over secp256k1. Version 2 replaces the fixed Euclidean schedule argument in version 1 with a finite polyhedral antinorm certificate. A machine-checked reconstruction proves the new quotient-weight bound of 405 and the resulting 1,620-step schedule. The published inverter still fails on valid inputs: its coefficient endpoint truncates a reachable operand, its active window omits a required secp256k1 position, its final remainder-length endpoint exceeds the work register, and terminal padding moves the inverse away from the stated output slice. A later companion revision changes each mechanism. Finite executions and formal reconstructions support those changes, while a circuit-level theorem for the complete measurement-enabled generator remains absent. A separately verified repair computes inversion for every nonzero reduced secp256k1 input, preserves the input, and clears its workspace. It uses 858 logical wires and has syntax-derived upper bounds of 2,209,345,754 reversible gates, 1,140,152,658 Toffoli gates, and 2,185,828,088 CNOT gates. The published affine point-addition schedule is correct only when its divisor and an internal multiplication operand are nonzero. Its coherent caller includes excluded group cases, so the published circuit does not establish total group translation. The paper’s asymptotic arithmetic is conditionally reproducible, but the current companion cannot reproduce its numerical rows, and the complete ECDLP width lacks a peak-live register allocation.

1 Artifacts and evidence

The audited publication is arXiv:2607.13816v2 and its TeX source archive [6]. The archive’s SHA-256 digest is

116c93984895a034fd097564b4bd29903874f19aa8cc41e30fd60f4587df9637.

The companion revision e64aa3c1198, dated 29 August 2026, postdates version 2 [5]. Its Git tree is

fd9fcfd1d68851c0108704d374447a94945d5f88.

Results about that revision describe later source changes. Published claims remain tied to version 2.

The formal evidence is VQ revision 9c3f249c062d, checked with Lean 4 4.32.0 and pinned library revisions [10, 1]. VQ represents reversible circuits by executable syntax and proves their basis-state action, preserved registers, workspace cleanup, coherent linear extension, and syntax-derived logical resources. Its hybrid-program semantics also covers measurement, reset, classical feed-forward, and branch-indexed resource use. The results in this report use exact arithmetic proofs, generated-circuit proofs, and hybrid-program proofs according to the claim under examination.

Table 1: Evidence classifications used in the audit.

Classification	Meaning
Exact mathematics	An arithmetic statement proved from integer, finite-field, or elliptic-curve definitions.
Generated-circuit theorem	A kernel-checked result about the action, cleanup, or resources of one stated reversible circuit.
Hybrid-program theorem	A kernel-checked result including measurement branches, reset, classical control, and phase correction.

Classification	Meaning
Finite source execution	Execution of pinned companion code on a stated finite domain through its bundled exact or sparse-state runtime.
Source inspection	A conclusion from formulas, register declarations, or construction order in pinned source.

A finite source test establishes the executed inputs and paths. A value-level field identity establishes arithmetic independently of a gate generator. Resource bounds in the formal artifact come from the same syntax named by the corresponding circuit theorem. The numerical audit of the companion follows its blockwise counting code and records the missing generated artifacts described in Section 9.

The standard quantum Fourier transform, observation law, and classical postprocessing in the elliptic-curve discrete-logarithm algorithm follow the cited Shor and Proos–Zalka constructions [8, 7]. This audit does not reprove those background results. Their application requires a coherent total group operation, which Section 8 assesses.

2 Results summary

Table 2: Verified results, faults, and repairs.

Area	Verified result	Gap or error	Repair or remaining work
Euclidean schedule	Quotient weight is at most 405, giving 1,620 phase steps. A lower bound of 256 limits terminal padding to 596 steps.	The paper prints the wrong sign for δ and inserts a spurious +1 in one quotient sum.	Corrected notation and the verified schedule support the repaired inverter.
Published and companion inverter	Exact traces establish the published faults. Formal reconstructions and finite source executions verify the later changes on their stated domains.	The coefficient endpoint, active window, final length endpoint, and terminal extraction fail. The later complete generator lacks a refinement and cleanup theorem.	The companion changes all four mechanisms. A separate full-register inverter has an end-to-end proof.
Repaired inverter	For every nonzero reduced secp256k1 input, the circuit produces its inverse, preserves the input, and clears the workspace. It uses 858 wires and at most 1,140,152,658 Toffolis.	Full arithmetic registers exceed the paper’s optimized resource claims.	The version 2 schedule reduces the earlier repair from 3,072 to 1,620 steps and from 860 to 858 wires.
Higher arithmetic	Proofs cover modular reduction, flag cleanup, doubling, halving, Horner multiplication, and coherent measured recycling under exact recomputation.	The squaring description aliases a selector and addend wire. The emitted optimized components lack the refinements needed by the recycling theorem.	The companion copies and clears each selector, adding two CNOTs per multiplier bit. Complete refinement remains open.
Point addition	The affine schedule is correct when the divisor and the later multiplication operand are nonzero.	Doubling, inverse pairs, infinity, and cases where $x_3 = x_2$ fall outside that domain.	A verified total repair covers all valid coordinate encodings with 12,319 wires and at most 1,218,141,048 Toffolis.
Resource claims	The layout sums and asymptotic component arithmetic can be reproduced under the paper’s component assumptions.	The complete 835-wire peak lacks an allocation proof, one subscript is wrong, one numerical exponent is inconsistent, and the current companion lacks the generated counting artifact.	The repaired inverter and total point adder have syntax-derived bounds. The optimized construction requires a complete operation stream and matching proofs.

3 Euclidean schedule

For every coprime pair (p, x) with 256-bit p and $0 < x \leq p/2$, the quotient weight is at most 405, and terminal entry occurs within 1,620 phase steps.

Algorithm 3 realizes each ordinary Euclidean quotient through four circuit phases. For a positive quotient q , define its binary weight

$$d(q) = \lfloor \log_2 q \rfloor + 1, \quad W = \sum_i d(q_i).$$

The first terminal state occurs after $N = 4W$ phase steps. A fixed quantum circuit therefore needs a universal bound on W for every allowed input, as well as correct behavior for the terminal suffix remaining before the fixed horizon.

Version 2 proves the required growth estimate with a polyhedral antinorm on the invariant cone

$$\mathcal{C} = \{(a, b)^T : a \geq b \geq 0\}.$$

For $M(q)(a, b)^T = (qa + b, a)^T$, set

$$\rho = 2 + \sqrt{3}, \quad \lambda = \rho^{1/3}, \quad F(v) = \min_{0 \leq j \leq 3} u_j v,$$

where

$$\begin{aligned} u_0 &= (\lambda^3 - 1, 1), \\ u_1 &= \left(\lambda^2, \frac{\lambda^3 - 1}{\lambda} \right), \\ u_2 &= \left(\frac{5}{\lambda} - \frac{1}{\lambda^4}, \frac{1}{\lambda} \right), \\ u_3 &= \left(\frac{6\lambda^3 - 1}{\lambda^5}, \frac{5\lambda^3 - 1}{\lambda^5} \right). \end{aligned}$$

These rows arise from the extremal alternating quotient pattern (1, 2) and two additional normalized images. This construction uses the extremal-antinorm method of Guglielmi and Protasov [3].

The machine-checked certificate proves

$$F(M(q)v) \geq \lambda^{d(q)} F(v) \quad \text{for every } q \geq 1 \text{ and } v \in \mathcal{C}.$$

For quotient bit lengths through four, a finite table shows that every normalized image of each supporting row dominates a convex combination of the four rows on $\mathcal{C}$. Exact algebraic-number inequalities establish all table entries. For larger quotients, monotonicity in q and the estimate $q/\lambda \geq \lambda^{d(q)}$ supply the bound. Iteration over the continuant product converts the quotient weight into growth of the initial modulus.

For a normalized input below half the modulus, the resulting inequality gives

$$W \leq \lceil cn \rceil, \quad c = \frac{3}{\log_2(2 + \sqrt{3})}.$$

Exact ceiling arithmetic yields $W \leq 405$ at $n = 256$, hence

$$N \leq 4 \cdot 405 = 1620.$$

For each $0 < a < p$, preprocessing replaces a by $x = \min(a, p - a)$, which satisfies $2x \leq p$. The formal result covers every coprime pair (p, x) obtained by this transformation when p has 256 bits, and connects the quotient-weight theorem to the first terminal state of the four-phase execution.

The same development proves the lower estimate

$$p < 2^W \gcd(p, x)$$

in the form required by the Euclidean trace. A coprime input for a 256-bit prime therefore has $W \geq 256$, so terminal entry occurs no earlier than step 1,024. At the 1,620-step horizon, the longest terminal suffix is

$$1620 - 1024 = 596.$$

Every terminal index and suffix is divisible by four. At suffix depth d , the later companion stores the low nine bits of $d - 1 \bmod 2^{10}$ in the shift word and the complement of bit nine in a reused epoch bit. The 596-step bound proves that this representation has sufficient capacity. It does not prove the emitted terminal circuit.

Two notation faults in version 2 leave this theorem unchanged. The active-window proof sets $\eta = ((4\sqrt{3} - 3)/13)\lambda^2$ and requires $\delta = -\log_\lambda \eta$. The printed section instead defines $\delta = \log_\lambda \eta$ while giving and using the positive value from the appendix. The overview also writes $\sum_i (d(q_i) + 1)$ once, whereas the definition and proof use $\sum_i d(q_i)$.

4 Published inverter faults

Published Algorithm 3 fails its universal nonzero-input interface: reachable traces exhibit coefficient truncation, missing active-window support, an out-of-register length endpoint, and incorrect fixed-slice extraction.

4.1 Coefficient routing

At a phase boundary, r and r' are the current Euclidean remainders, t and t' are their nonnegative coefficient magnitudes, and q is the partial binary quotient. They satisfy

$$rt + r't' + qr't = p.$$

The variables ℓ_t and $\ell_{r'}$ record the bit lengths of t and r' , while ℓ_s records the cyclic displacement of the second work field. The pair $(\text{phase}_1, \text{phase}_2)$ selects one of the four microsteps used to process a quotient bit.

The two shared $(n+3)$ -position work fields contain coefficients, quotient data, and remainders. A shift counter rotates the second field, so the live boundary of its adjacent remainder determines the coefficient operand in phase $(1,1)$. The published coefficient block instead uses the first $\ell_t + 1$ positions for both coefficient operands. The length ℓ_t describes the first coefficient and does not bound the shifted coefficient in the second work field.

The normalized trace for $(p, x) = (251, 3)$ reaches, before step 27,

$$t = 1, \quad q = 0, \quad r = 2, \quad t' = 83, \quad r' = 3,$$

$$\ell_t = 1, \quad \ell_{r'} = 2, \quad \ell_s = 2, \quad (\text{phase}_1, \text{phase}_2) = (1, 1).$$

The coefficient relation $2 \cdot 1 + 3 \cdot 83 = 251$ confirms the state. Full arithmetic reads $t' \gg 2 = 20$. The published two-position slice reads $20 \bmod 4 = 0$. Its subtraction produces a borrow absent from the full-width operation, and the phase successor differs from Algorithm 3. Finite evaluation checks reachability of the state and exact action of both arithmetic interpretations.

The published active-window formula fails independently at cryptographic width. For secp256k1 input $x = 2^{224} - 1$, the reference trace reaches the following phase- $(1,1)$ state before one-based step 128:

$$t = 1, \quad r = 2^{224} - 978, \quad t' = 2^{32} - 1, \quad r' = 2^{224} - 1,$$

$$\ell_t = 1, \quad \ell_{r'} = 224, \quad \ell_s = 1.$$

The complete live interval ends at position $(n+3) - \ell_{r'} - \ell_s = 34$. The published bound gives

$$K_3(128) = \min(\lceil 128/4 \rceil + 1, 257) = 33.$$

Position 34 is therefore absent from the generated block. The endpoint fault can truncate a supplied interval. The window fault can omit a required position before endpoint selection. Each needs its own repair.

4.2 Remainder-length update

The final ordinary division produces successor remainder zero. In the paper's length encoding, a w -bit word stores $L - 1 \bmod 2^w$ for decoded length L . The all-ones word represents $L = 0$. The final zero remainder has logical upper endpoint $n+4$. The physical work field has positions through $n+3$. Thus the final remainder-length writer addresses one position beyond its declared register. The $(37, 13)$ trace reaches this case at one-based step 32.

The later companion caps the physical endpoint at $n+3$. A formal reconstruction proves that the capped suffix writes the zero encoding, stays inside the declared register, and restores its decoder workspace. The proof also covers positive successor remainders. This repair changes the published length-window construction and its exact resource count.

4.3 Terminal extraction

The four-phase circuit continues executing after the Euclidean recurrence has terminated. Each terminal step rotates the second work field and increments the shift state while preserving the decoded Euclidean values. A fixed physical output slice therefore depends on how many padding steps follow the first terminal state.

The paper's $(p, x) = (37, 13)$ trace returns 4 from the stated fixed slice, while the inverse is 20. The first terminal state occurs at step 32 with coefficient $t' = 17$ and shift zero. The table continues through step 36,

adding four rotations to the nine-position field. The set bits of 17 move so that the low six physical positions contain 33. Copying that slice and applying the recorded sign correction yields

$$37 - 33 = 4.$$

The modular products confirm the discrepancy:

$$13 \cdot 20 \equiv 1 \pmod{37}, \quad 13 \cdot 4 \equiv 15 \pmod{37}.$$

The formal evidence checks the complete fixed-horizon trace, the physical slice, and both modular products. The corrected schedule in Section 3 changes the horizon and leaves the extraction defect intact.

Each counterexample lies on a valid inversion trace. The coefficient fault changes a live transition, the length update exceeds the physical layout, and terminal extraction can return a noninverse after the live recurrence has finished. Resource formulas based on the published windows count syntax that does not implement the stated map.

5 Post-publication companion

Companion revision **e64aa3c1198** changes the four mechanisms identified above. Its phase-(1,1) coefficient endpoint uses $n + 3 - \ell_{r'} - \ell_s$, while phase (1,0) retains the endpoint derived from ℓ_t . Its coefficient window becomes $\min(\lfloor T/4 \rfloor + 2, n + 1)$, supplying position 34 at step 128. The length update caps the zero-remainder endpoint at the end of the work field.

Terminal padding uses the representation defined in Section 3. Each padding step rotates the second work field and increments the encoded depth modulo 2^{10} . The wrapper later restores the work-field orientation from the complete terminal shift. It then compresses the epoch through a three-bit code formed from the two low encoded depth bits and the complemented high bit, extracts the coefficient, and applies an explicit inverse sequence for cleanup. Reachable four-step-aligned suffixes give code 011 or 111. The compression fixes 011 and exchanges 111 with 000. The 596-step maximum terminal suffix fits within the 1,024 counter states.

Formal reconstructions establish the arithmetic content of the changed mechanisms. The proved results cover both coefficient endpoints, containment of coefficient and length windows under stated trace invariants, capped zero-remainder decoding, terminal rotation, low-counter increment, temporary storage of the epoch in the zero-encoded quotient-length bit, restoration of the work-field orientation with the swap order emitted by the companion, epoch compression, coefficient extraction, inverse cancellation, and scratch cleanup. A recursive reconstruction proves that the companion’s truncated binary-tree selector activates exactly the positions from the window start through the decoded endpoint and implements addition or subtraction on that prefix for every coefficient-window size used at secp256k1. These are theorems about specified reconstructed circuits. Syntax identity and semantic refinement of the complete public generator remain open.

We ran the pinned source through its bundled exact reversible and sparse-state runtimes on the domains in Table 3. Qiskit was absent from the test environment. We installed no substitute dependency.

Source execution	Result
Euclidean steps	Every nonzero input at $p = 251$ and $p = 419$ matched an independent reference recurrence at every live step, including packed work fields, lengths, phases, signs, parity, and cleared auxiliaries.
Binary-tree selector	The binary-tree selector matched direct fixed-interval arithmetic on 15,360 basis configurations over five- and nine-position windows.
Terminal padding	Every four-step-aligned suffix through 596 passed. Suffixes of lengths 4, 508, 512, 516, and 596 also passed complete forward-inverse cleanup.
Point addition	68 eligible cases over fields 13, 17, and 31 passed within the nonzero affine domain.
Measured execution	Eight sparse trajectories for a two-branch field-13 state preserved the expected relative phase and cleared the declared workspace.

Table 3: Finite executions of companion revision **e64aa3c1198**.

The finite executions exclude zero denominators, zero internal multiplication operands, infinity, inverse pairs, and doubling. Their measurement coverage consists of the eight sparse trajectories in Table 3. Formal reconstructions and source executions verify the listed mechanisms and finite domains. The complete measurement-enabled circuit lacks a semantic refinement and cleanup theorem.

6 Repaired inverter

The verified replacement uses complete arithmetic windows and the 1,620-step schedule. For the secp256k1 modulus [9], it accepts every integer a satisfying $0 < a < p$, preserves a , writes the unique reduced b satisfying

$$ab \equiv 1 \pmod{p},$$

and restores every workspace bit to zero. The theorem covers the generated reversible circuit and therefore extends coherently from basis states to superpositions of allowed inputs.

The circuit prepares the Euclidean encoding from the plain source register, runs the normalized fixed schedule, cancels the terminal physical shift before coefficient extraction, applies the sign correction, copies the reduced inverse to a separate output, reverses the Euclidean execution, and reverses input preparation. The cleanup theorem covers the encoded work fields, length and phase data, selector scratch, arithmetic scratch, and preparation workspace. The result uses no measurement or reset, and its syntax establishes the independent upper bounds in Table 4. The gate-class bounds are not a partition of the total bound. Each is a separately proved inequality.

Resource	Verified bound
Peak logical wires	858
Reversible gates	$\leq 2,209,345,754$
Toffoli gates	$\leq 1,140,152,658$
CNOT gates	$\leq 2,185,828,088$
Measurements, resets, and classical operations	0

Table 4: Syntax-derived resources for the repaired plain-input secp256k1 inverter.

The antinorm schedule improves the same full-window repair over its general $12n$ schedule. The earlier schedule uses 3,072 rounds and a 12-bit terminal shift field. The new schedule uses 1,620 rounds and an 11-bit field. The checked comparison reduces width from 860 to 858 and strictly reduces each gate bound. The corresponding 3,072-round caller bounds are 8,515,841,972 reversible gates, 2,162,792,474 Toffolis, and 4,144,899,036 CNOTs.

Complete windows make the verified replacement much larger than the paper’s optimized in-place inverter: the published width formula evaluates to 579 at $n = 256$, whereas the repair uses 858 wires and a separate output.

7 Multiplication and measured recycling

The modular-multiplication arithmetic in Appendix B is correct at the mathematical-value level after separating the squaring selector from the addend register. Let $a, z < p$, let $s = a + z$, let $w = s \bmod 2^n$, and let o denote the word-overflow bit. The checked reduction identity is

$$o \text{ xor } [w \geq p] = [s \geq p].$$

Conditional subtraction of p therefore returns $s \bmod p$. The final comparison of the corrected result with the addend reconstructs the controlled reduction flag, allowing exact uncomputation. Separate proofs establish that modular halving reverses modular doubling for an odd modulus and that the high-to-low double-and-add recurrence returns the Horner value of the decoded multiplier.

The published squaring description uses a multiplier bit both as the selector of a controlled addition and as a bit of its addend. The controlled-adder cells require distinct control and data wires. The post-publication companion copies each selector into a clean bit, performs the controlled addition, and uncopies it. This repair adds two CNOTs per multiplier bit and no Toffoli gates. It changes exact CNOT counts while preserving the stated leading Toffoli coefficient.

The measurement-assisted register-recycling argument has a general hybrid-program proof. Suppose a reversible computation can reconstruct the obsolete field exactly from the retained fields. Measuring the obsolete field in the Hadamard basis records a parity-dependent phase. Reset removes the measured data. Exact recomputation, classical phase correction from the measurement record, and reverse recomputation cancel that phase and clear the temporary field on every branch. The resulting channel preserves the coherence of the retained state. This theorem formalizes the uncomputation method used in measurement-assisted arithmetic [2].

Application to the emitted Figure 15 circuit still requires exact refinements from its optimized inverter and multiplier generators to the reversible maps assumed by the hybrid theorem. The companion executions in Table 3

check selected trajectories. They do not replace the missing program theorem for all basis states, amplitudes, measurements, and cleanup branches.

8 Point-addition domain

The published Figure 14 schedule implements an affine addition only when its division operand and later multiplication operand are nonzero.

Figure 14 implements the generic affine formula for adding $P_1 = (x_1, y_1)$ and the fixed point $P_2 = (x_2, y_2)$:

$$\lambda = \frac{y_1 - y_2}{x_1 - x_2}, \quad x_3 = \lambda^2 - x_1 - x_2, \quad y_3 = \lambda(x_1 - x_3) - y_1.$$

A field-level reconstruction proves the stated result when the division and multiplication subroutines receive nonzero first operands. It also proves that the schedule restores its input when the external control is zero.

The division occurs before the controlled coordinate correction and receives $x_1 - x_2$ in both control sectors. Even the clear-control branch therefore requires $x_1 \neq x_2$. The enabled branch later presents $x_2 - x_3$ as the first operand of the in-place multiplier and requires $x_3 \neq x_2$. These conditions require distinct input x -coordinates and a result whose x -coordinate differs from the addend's. The paper states interfaces only for components with nonzero first operands but gives Figure 14 no matching domain restriction.

Equal input x -coordinates cover doubling and inverse pairs and make the division operand zero. Infinity also lies outside the affine register model. The equality $x_3 = x_2$ can occur after a valid division. For example, with the secp256k1 generator G , adding G to $-2G$ yields $-G$. The result and the addend have the same x -coordinate, so $x_2 - x_3 = 0$ at the multiplier call. This ordinary group addition violates the component premise.

A signed-window quantum scalar multiplication applies controlled additions coherently across basis values of the scalar register [4]. Its state space includes doubling, inverse-pair, infinity, and branches where $x_3 = x_2$. The unchanged companion point-addition builder contains no exceptional-case selection. The ECDLP caller requires total controlled group translation across those excluded branches.

A separate verified repair uses $(0, 0)$ for infinity and reduced affine coordinates for finite secp256k1 points. It handles the exceptional cases, restores its workspace, and implements controlled translation on every valid coordinate encoding. Its peak width is 12,319 logical wires, and its Toffoli count is at most 1,218,141,048. Those resources describe the total repair.

9 Resource claims

9.1 Logical width

The verified 835-wire figure applies to one controlled point-addition layout, while the complete ECDLP peak has no register-allocation proof.

The published inversion formula is

$$2n + 6\lceil \log_2 n \rceil + 19.$$

At $n = 256$ it gives $512 + 48 + 19 = 579$ logical wires. The current companion's shared Euclidean layout declares two 256-wire work fields and 66 auxiliary wires, for 578. The source changes the terminal representation and allocation, producing a width that differs from the published formula. The published circuit faults remain.

The published point-addition formula is

$$3n + 6\lceil \log_2 n \rceil + 19,$$

which gives $768 + 48 + 19 = 835$. The current companion constructs the same total as three 256-wire coordinate/work fields, 66 shared auxiliaries, and one external point-addition control. This verifies the declared register-layout count for one controlled affine point-addition call. Functional correctness and peak width of its caller require separate proofs.

The complete ECDLP construction later uses a signed-window lookup with $w = 16$. Its point-adder interface receives 16 sign-and-address bits. The 835-wire layout allocates one control wire. Retaining all 16 bits in place of that control would add 15 live wires. Reuse requires an explicit lifetime and allocation argument. The paper provides no peak-live allocation containing the window bits, lookup state, point-addition workspace, measurements, and feed-forward data within 835 wires. The 835 count therefore applies to the point-addition layout shown in the companion.

9.2 Asymptotic gates

Summing the paper’s listed inversion components reproduces

$$(160c - 36)n^2 + O(n \log n) \quad \text{Toffolis}$$

and

$$(200c - 42)n^2 + O(n \log n) \quad \text{CNOTs},$$

where $c = 3/\log_2(2 + \sqrt{3})$. The coefficients evaluate to 216.6357505 and 273.7946881. The text rounds these to 217 and 274.

The interval $[k_4(T), K_4(T)]$ is the active range of the ℓ_t length writer at step T , and $[k_5(T), K_5(T)]$ is the active range of the $\ell_{r'}$ writer. One intermediate line uses $K_4 - k_4$ for the $\ell_{r'}$ contribution. The component table and the derived coefficient require $K_5 - k_5$. Correcting that subscript reproduces the displayed total. The counterexamples invalidate the published coefficient endpoint, coefficient window, and zero-remainder endpoint. The arithmetic check remains conditional on those component formulas.

Under the same component assumptions, four inversion passes, six modular multiplications, and two squarings yield

$$4(216.636) + 6(17) + 2(17) < 1003$$

as the leading Toffoli coefficient for one point addition. With $w = 2\log_2 n$, five 2^w lookup charges per window, and $2n/w$ windows, the paper obtains

$$1008 \frac{n^3}{\log_2 n} + O(n^2).$$

These sums are arithmetically consistent. Their application assumes a total point adder and the published optimized component syntax. The faults and repairs above invalidate those premises.

9.3 Numerical counts

The companion’s numerical counter compiles reusable blocks, stores their counts, and assembles larger totals from declared multiplicities. The current revision contains no canonical point-addition operation stream. Its main row requires a generated 256-bit Algorithm 3 count file, which is absent from the repository.

The post-publication generator changes coefficient windows, boundary arithmetic, terminal controls, epoch handling, extraction, and inverse cleanup. Counts from an earlier generated file would therefore describe different syntax. Reproducing the 30.59-million-Toffoli inverter row and 70.10-million-Toffoli point-addition row requires regeneration of the missing component and proofs for the identities and multiplicities of the assembled blocks. The numerical table remains an unverified artifact result.

The paper’s complete secp256k1 formula uses 28 signed-window additions, five 2^{16} lookups per addition, and $Q_A = 70.10 \times 10^6$ Toffolis per point addition,

$$28(5 \cdot 2^{16} + 70.10 \times 10^6) = 1,971,975,040.$$

Its base-two logarithm is 30.877, agreeing with the introduction’s $2^{30.88}$ after rounding. Section 6.4 reports $2^{30.63}$ for the same substitution, which is inconsistent with the displayed formula and table row.

10 Remaining verification

The current companion circuit needs one theorem connecting its emitted measurement-enabled inverter, multiplier, and cleanup operations to their mathematical maps. That theorem must cover every branch, classical record, phase correction, reset state, and restored scratch field. A canonical operation stream bound to the source revision would then support resource counts from the same artifact.

A low-width complete ECDLP result also requires total controlled point addition. Exceptional-case selection must cover doubling, inverse pairs, infinity, and branches where $x_3 = x_2$ while preserving coherence and clearing its selectors. The complete signed-window circuit then needs a peak-live register allocation covering lookup addresses, loaded constants, point-addition workspace, and measurement records.

The final composition would join total double-scalar multiplication with the Fourier, observation, and classical-recovery stages. Functional correctness, success probability, width, and gate counts must refer to that same complete circuit. The published version and current companion do not yet provide this joined result.

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